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SIMULATION OF LIFE TESTING PROCEDURES FOR ESTIMATING LONG-TERM DEGRADATION AND LIFETIME OF AlGaN/GaN HEMTs (Postprint)

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14. ABSTRACT
Thermometry and thermo-mechanical: MicroRaman has been used both to track the thermal signatures as devices degrade and to assess the strain evolution within the devices during operation. It was found that both the piezoelectric and thermo-elastic strains decrease the overall strain (reduce the residual strain in the film), with the latter having the greater effect.

Modeling: Work has initiated on an improved thermal model that takes into account phonon scattering dynamics. Existing Fourier-based models underpredict the hot spot temperature.

Irradiation experiments: Radiation is being explored as a means to controllably damage a device to better understand how specific defects impact performance and lifetime.

15. SUBJECT TERMS
Degradation, FETs, GaN, GaN/AlGaN, HEMTs, HFETs, life estimation, life testing, MODFETs, reliability, simulation, thermal characterization, thermal resistance

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Simulation of Life Testing Procedures for Estimating Long-Term Degradation and Lifetime of AlGaN/GaN HEMTs

Eric R. Heller

***Abstract*—Finite element 3-D thermal simulations of long-term degradation in AlGaN/GaN HEMTs for high-power applications are reported on, in which temperature evolves over time as the *local* degradation rate varies within the modeled device based on the local temperature of the degrading region (i.e., the channel). Specifically, hotter regions within a device are modeled as degrading faster due to a thermal component to the degradation rate equation. This allows self-consistent simulation of life testing, commonly used to estimate long-term reliability by extrapolating failure times seen at elevated channel temperatures to a lower "use" temperature. We find that it is necessary to consider the entire distribution of temperatures within the device instead of at one characteristic location to get the most accurate estimates for long-term device life. The effect of device geometry, assumed degradation mode, incorrect thermal resistance data, and dissipated power level on this lifetime estimation error is investigated. It is found that the error in the extrapolated failure time is greatly increased when both the thermal resistance is in error and the dissipated power of the life test does not match the expected power during operation, compared to when only one of these is off.**

***Index Terms*—Degradation, FETs, GaN, GaN/AlGaN, HEMTs, HFETs, life estimation, life testing, MODFETs, reliability, simulation, thermal characterization, thermal resistance.**

I. Introduction

FOR high-power-density applications, AlGaN/GaN HEMTs have been identified as very promising devices [1]. Because of the high-power capability and high-temperature survivability of this materials system, groups have designed devices that reach very high channel temperatures $(T_{\rm ch})$ in operation [2]–[4]. $T_{\rm ch}$ can easily be 100 °C or more above baseplate temperature and can vary greatly from the center of a central finger of a large multifinger device to the edge [2]–[4].

A common method of estimating the long-term operating lifetime of an AlGaN/GaN HEMT for power radio-frequency (RF) amplification is to conduct a "life test," where several (typically three) populations of devices are run at different baseplate temperatures with otherwise similar operating conditions. The devices are run until some failure criterion is reached, which, for a dc test, is usually some drop such as 10% in the drain saturation current $I_{\rm DSS}$ and, for RF testing, is typically a certain drop in RF power or operating efficiency. Higher temperatures generally lead to shorter time to failure, and the data are commonly fitted to a thermal Arrhenius activation energy model for the failure mode responsible for the degradation, where the temperature required in the model is that of the failing region [5]. This Arrhenius activation energy is used to extrapolate the measured lifetimes and find the expected lifetime of the device at the baseplate temperature expected during operation, by extrapolating this temperature to that of the same region that was known to fail.

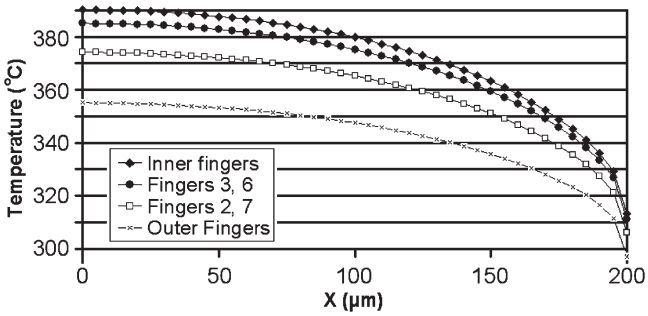

Fig. 1. Temperature along the gates (at the center of the bottom of each gate) for a representative 8×400 μm device with 25-μm spacing between gates running at $V_{\rm DS} = 10$ V and $V_{\rm GS} = 0$ V, and temperature at the baseplate of 200 °C. Due to symmetry, only data for half of the fingers and for half of their length are shown.

The long-term failure of a *good* device is commonly attributed to degradation over the entire device structure. This may lead to a sudden destructive run-away event at one point, but it is assumed that the device was fairly uniform in initial properties at the start of operation and that there was no initially weak point that drove the initial degradation. Of course, the device is not at a single uniform temperature during the high-power operation required for testing these devices. Specifically, for the typical large device, the important regions of the device (i.e., channel, gate, source, drain) will be hottest in the center of the device and cooler at the edges, as shown in Fig. 1 [2].

Because of this and due to the temperature-dependent degradation rate assumed in the Arrhenius model, the local degradation rate is expected to vary with position over the device. Traditional failure analysis does not take this into account but uses a single estimated value for the peak temperature. Device modeling will be used to explore how the data extracted from the Arrhenius model changes when this assumption is made compared to when it is not. As time progresses, degradation is seen to change the power distribution within the device, and

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both this and the resulting evolution of temperature with time are modeled. In addition, temperature varies greatly over the source–gate–drain (S-G-D) region, as shown in an earlier work [2] that is built on here and also experimentally by Micro-Raman in [3]. Along the channel, temperature typically peaks at a submicrometer-sized region at the drain edge of the gate where the device is pinched off, but it is not easy to get this exact temperature [2]–[4]. It is expected that the failing region is along the gates where the temperature is highest, and so, this temperature is used for the failure determination in this publication, although it will be briefly mentioned how data extracted from the Arrhenius model change when the region responsible for the degradation changes.

Also to be explored is the change in the thermal conductivity with temperature of some of the materials that GaN HEMTs are composed of, specifically SiC and GaN. Of course, this makes the thermal resistance of the device temperature dependent, and it will be shown through device modeling that this temperature dependence should not be ignored when adjusting the baseplate temperature during a life test. If it is, it can lead to an estimate of the activation energy that is considerably higher than the true value, because a given increase in the baseplate temperature can lead to a much greater increase in the temperature at the failure region. Overestimating the activation energy for failure leads to overly optimistic operating lifetime predictions.

II. Model

To model these effects, a representative eight-finger, 400-μm gate width, and 25-μm gate pitch device has been modeled in the finite element program ANSYS [6], along with variations such as two fingers instead, 150-μm gate width, 35-μm gate pitch, etc. The GaN was 1.2-μm thick, the SiC substrate was 350 μm (or 175 μm in one case), and the SiC simulation domain is 2 mm $\times$ 2 mm, chosen to be large enough so that further increases do not change the model results significantly [2], [7]. All boundary conditions are adiabatic except for the bottom of the SiC substrate, which is fixed. Because of fourfold symmetry, only one-fourth of the device is modeled, for example, as four 200-μm fingers with adiabatic boundary conditions at the reflection planes. Because of degradation, the local power dissipation in the device cannot be assumed as constant along the gate width but is assumed to vary with position and is loaded into an initial data file. Temperature-dependent thermal conductivities have been used for GaN and SiC [8] that have been previously reported in the literature and seen in our prior modeling efforts [2] to reproduce the micro-Raman results of Kuball *et al.* [3]. For GaN, this prior work had used the form in [9], but for this work, $1.6 \times (T/293\ \mathrm{K})^{-1}\ \mathrm{W}/(\mathrm{cm}\cdot\mathrm{K})$ was used as per [3], which we believe may better reflect the temperature dependence of the GaN thermal conductivity at high temperatures. Either form was seen to give the same qualitative conclusions. Moreover, it is known that the interface between GaN and SiC will have a low thermal conductivity due to high defect density, also known as a thermal boundary resistance [10]–[12]. There is a large variation in the reported values of this resistance, and so, for simplicity, this effect has been neglected here. Fortunately, it is not the absolute temperature but the difference in temperatures along a device that produces the errors investigated in this model, and the model has been found fairly insensitive to changes of this nature.

The thermal model has been set up to compute and store the temperature as a function of the position along the gate width of each finger for this arbitrary power distribution data file that was mentioned. Instead of one global temperature driving degradation, it is assumed that there is one point within a plane along the S-G-D cross section that is representative of the position of the fail region, and this temperature is what is recorded for local degradation rate modeling. The power distribution data (i.e., $V_{\mathrm{DS}} \times I_{\mathrm{DS,local}}$) that were used by ANSYS and the temperature distribution data are both loaded into a separate utility, and power degradation is computed by a user-defined formula. For all of the simulations that were run for this work, this rate was assumed to be given by

$$P(x,n,t+\Delta t) = P(x,n,t) \Big/ \left(1+\Delta t * A e^{-E_a/k_b T(x,n,t)}\right) \quad (1)$$

where Δt is a time step that is small enough that the degradation rate is roughly constant during its duration (i.e., the power would follow a decaying exponential with time if T was held constant), P is the local power dissipation at one place measured along the gate width (which extends along x) for finger n, T is the local temperature at the region where the failure mode is assumed to take place (for example, the center of the bottom of the gate), and A and E_a are the prefactor and Arrhenius activation energy for the degradation, respectively. Data for this time step are archived, time is incremented, and the power distribution table is recomputed using (1). ANSYS can now be used to compute new temperatures, and this cycle is repeated to the end point time where the degradation has progressed to failure. For some simulations where the baseplate temperature is adjusted during the run, the baseplate input temperature used in ANSYS is adjusted once per time step. Alternatively, some simulations were run where the total power was held constant by effectively adjusting the gate voltage; this is probably more common than is baseplate adjustment for dc life tests of GaN HEMT devices. In this case, first, (1) is used for power degradation, and then, local power is adjusted to restore the total power.

Since the S-G-D spacing over which the high electric fields exist and in which the device current flows is typically $\sim$5 μm and not as deep, we assume for our modeling effort that the physics of device failure (i.e., trap generation or a similar process) operate in the micrometer or smaller size scale, and degradation effects at one place in the device do not directly affect another place much farther away on this finger or on another finger. For reference, the gate width is typically $\sim$150–500 μm, and the pitch between successive gate fingers is typically $\sim$25 μm. Of course, there are indirect effects that are included in the modeling effort. Degradation in one place will affect the current flow and may force changes on the gate or drain voltages externally applied to the whole device depending on the testing protocol in place. Also, local power dissipation creates heat that diffuses through the entire device.

The ideal power distribution will have slightly less power density in the center due to higher device temperatures there.

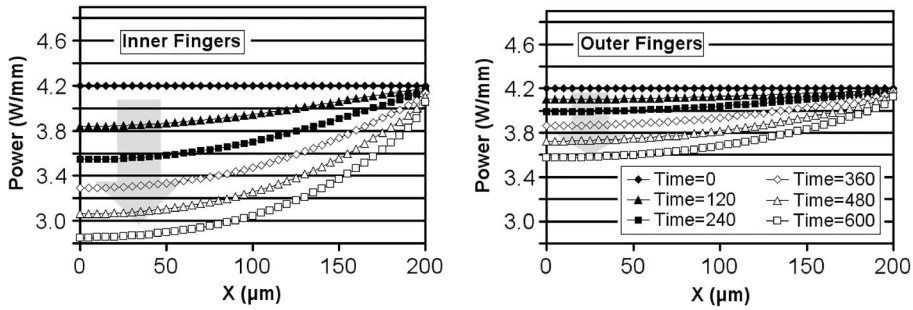

Fig. 2. Power as time (hours) progresses for an 8×400 μm initial 200 °C baseplate temperature device starting with an initial power of 4.20 W/mm, typical of a HEMT running at $V_{\rm DS} = 10$ V and $V_{\rm GS} = 0$ V at this elevated temperature. For clarity, only the two inner fingers and the two outer fingers are plotted. In (1), $A = 2 \times 10^8$ and $E_a = 1.5$ eV, and the temperature used for $T_{\rm fail}$ is at the center of the bottom of the gate.

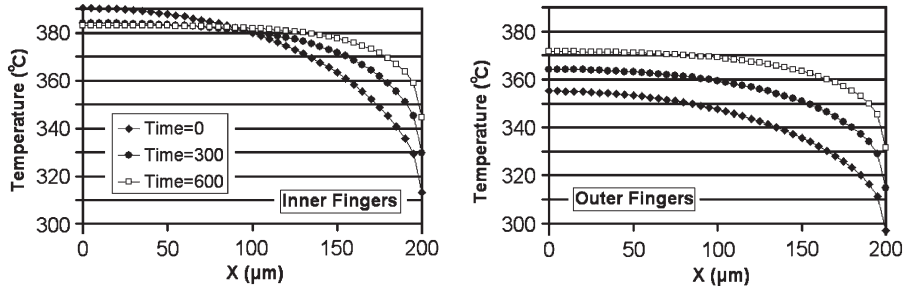

Fig. 3. Temperature as time (hours) progresses for the same device and simulated test as in Fig. 2, with the temperature at the center of the bottom of each gate plotted. The device runs from -200 to $+200$ μm. Baseplate temperature was adjusted up based on $R_{\rm th}$ for the center of the inner finger at $t = 0$; the more rapid degradation in the device center causes the temperature to drop, as shown there.

We expect power to vary as $\sim 1/T\hat{}\{n\}$ (T in kelvins) with $n \sim 0.6$ for a mostly closed channel [2]. This power distribution was modeled and found to not be a significant source of error, as will be discussed. Therefore, for simplicity, the initial power density has been assumed constant for most of the results reported.

Last, the thermal profile within a device can vary to some degree with the bias used to achieve a given power dissipation. For example, a fully open channel device has heating through the entire channel and also from contact resistance, while heating for a pinched off channel is focused on the pinch-off region, even when the total power is conserved. It is only reasonable to assume that degradation can affect this temperature profile as well, as will small changes in $V_{\rm GS}$ to adjust the total power, both of which will then affect the degradation rate. These effects could vary with the physics of the degradation mechanism and are beyond the scope of this paper.

III. Results

Fig. 1 shows the initial temperature distribution along the gates of the simulated device. Figs. 2 and 3 show the power degradation and the temperature profiles observed when a device is allowed to degrade based on the procedure outlined earlier. The device baseplate temperature is 200 °C at time $(t) = 0$. At $t = 0$, the full initial power is supplied to the device. Temperatures are highest in the center of the centermost fingers, and so, power degradation is greatest here. Likewise, degradation is slowest at the edges of the device, and in this example, the initial degradation at the far edge is $\sim$1.5% of the rate in the center. Degradation has been allowed to progress for a $\sim$19% drop in total power (beyond typical failure limits) to show trends. To more realistically simulate a life test, the baseplate temperature has been continually adjusted up to try to keep the channel at a uniform temperature, as may be done experimentally. This is typically done by measuring or otherwise determining the temperature rise over the baseplate temperature for the desired power level at the assumed "failing" region and computing a "thermal resistance" $R_{\rm th}$ by dividing by the power. In practice, this can only be done approximately because, as was shown, the device has a considerable temperature variation. The typical way to approximate this experimentally is to compute $R_{\rm th}$ between the center of one of the middle fingers (the hottest place) and the baseplate, and dividing by the *total power dissipation* $(P_{\rm tot})$ of the device, even though this is not the same as the local power dissipation. The failing region (often assumed to be the channel) temperature $T_{\rm fail} = T_{\rm base} + R_{\rm th} \times P_{\rm tot}$ is then held constant by adjusting $T_{\rm base}$ as $P_{\rm tot}$ decreases, where

$$T_{\rm fail} = T_{\rm base} + R_{\rm th} \times P_{\rm tot}. \tag{2}$$

In reality, the thermal resistance is a function of $T_{\rm base}$, $P_{\rm tot}$, actual device bias, local power dissipation, etc., but this is often neglected. Fig. 3 shows the resulting temperature profile when duplicating this procedure with the model; the baseplate temperature was raised from 200 °C at $t = 0$ to 236.3 °C at $t = 600$ h to keep $T_{\rm fail}$ constant based on (2). It is shown that, in reality, the temperature varies greatly, even in the center of the middle finger, and in this case, the average channel temperature increased by 17 °C.

Fig. 4 shows the same device as in Fig. 2, under the same initial conditions. In this case, instead of adjusting $T_{\rm base}$ for

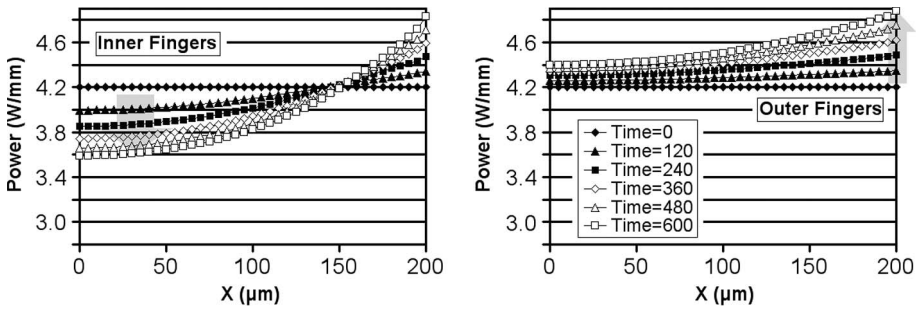

Fig. 4. Power as time (hours) progresses for a device similar to Fig. 2 and for the same initial conditions, except that, instead, the power is held constant by adjusting $V_{\rm GS}$, and baseplate temperature is a constant 200 °C.

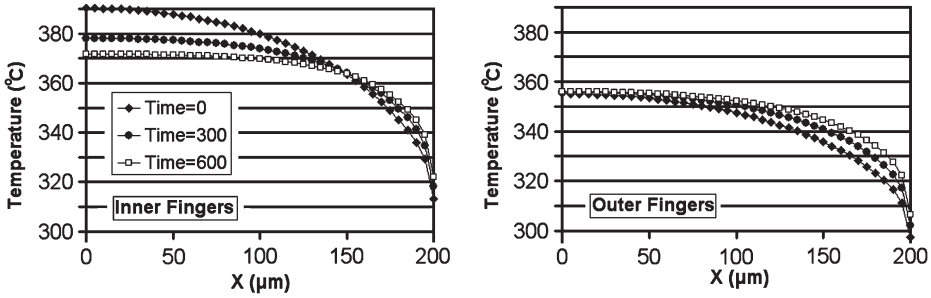

Fig. 5. Temperature as time (hours) progresses for the same device and simulated test as in Fig. 4.

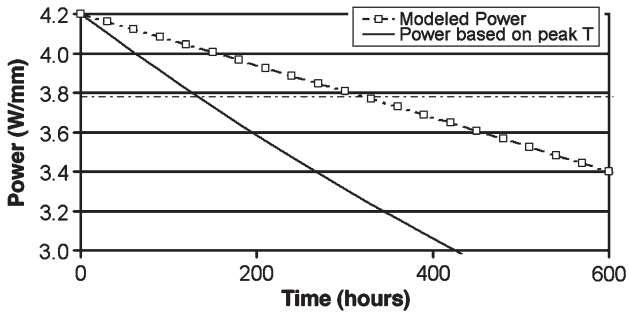

Fig. 6. Degradation of *average* device power shown with time for $E_a = 1.5$ eV and $A = 2 \times 10^8$ with 200 °C starting baseplate temperature. Triangles show the degradation based on the modeled temperature profiles of Fig. 5, and the line without data points shows the rate computed, assuming that the entire failure region is at $T_{\rm fail}$. The thin dash-dotted line shows the 10% power degradation point.

$t > 0$ degradation, $P_{\rm tot}$ has been held constant by adjusting $V_{\rm GS}$ so that $T_{\rm fail}$ and $T_{\rm base}$ both remain constant. For now, it is assumed that changes in $V_{\rm GS}$ scale all portions of the device up or down in power by the same percentage. This assumption will be discussed in more detail later. Fig. 5 shows the resulting temperature profile for Fig. 4. The final temperature device temperature is everywhere cooler than before, despite the same $T_{\rm fail}$ goal, and *the center changes far more than before*. However, this time, the average channel temperature was much more constant and decreased by only 1 °C. *If the temperature were monitored by some means that extracts an averaged temperature, the user would wrongly think the temperature did not change during the life test.*

Fig. 6 shows the modeled device power degradation (line with data points) based on the temperature profiles in Fig. 3 versus the expected degradation when it is assumed that $T_{\rm fail}$ accurately reflects the temperature of the entire failing region as is commonly done (plain line). In this case, $T_{\rm fail} = T_{\rm base} + R_{\rm th} \times P_{\rm tot}$ is 200 °C + 0.04530 × 4200 = 390.3 °C. The simple one-temperature model yields a faster degradation rate because $T_{\rm fail}$ was based on the hottest part of the gate finger (see Fig. 3). Of course, A and E_a are determined based on the values that fit the observed degradation rate and not the other way around. The point of Fig. 6 is to show how a given choice of A and E_a affects the simulated degradation and that A and E_a extracted from degradation data will be different when different channel temperature assumptions are made.

As mentioned, the ultimate goal of the life test is to find the Arrhenius activation energy E_a and prefactor A for the devices under test, and this cannot be done exactly when the temperature of the failing region drifts during the test. To determine the extent of this error through modeling, the simulated life test must be run for at least two temperatures, then separately corrected for the power degradation for each using the drop in average power as a guide (as done experimentally), and finally extract E_a' and A' using only the total power degradation as must be done experimentally. In all cases, 10% drop in total power is considered a failure. These quantities are primed to differentiate them as output values, separate from the inputs used in (1). In this case, the same procedure was repeated at $T_{\rm base} = 180$ °C. At each temperature, the "exact" $R_{\rm th}$ is extracted from the thermal model at the device finger center at $t = 0$, and in a sense, this is modeling the "ideal" experiment without measurement errors in $R_{\rm th}$. Fig. 7(a) and (b) shows the results, where $E_a' = 1.526$ eV and $A' = 1.30 \times 10^8$ are extracted by matching the time for 10% power degradation at this temperature and simultaneously for $T_{\rm base} = 180$ °C. This contrasts with the inputs $E_a = 1.500$ eV and $A = 2.00 \times 10^8$.

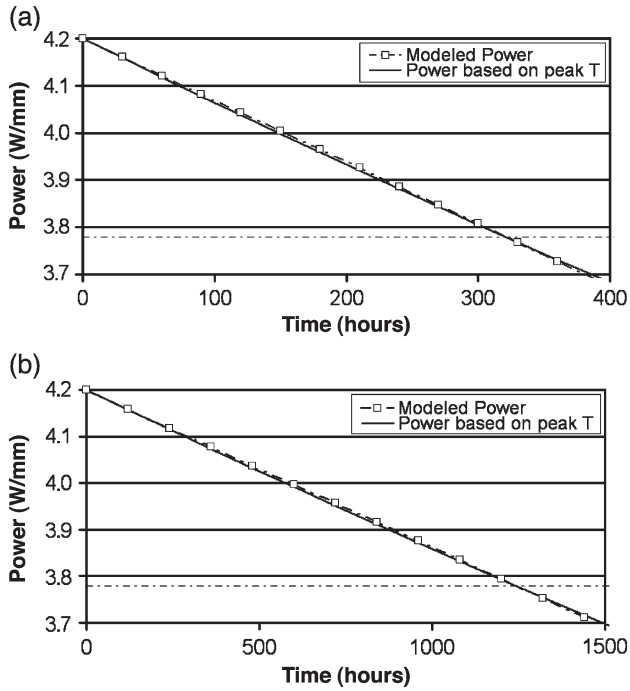

Fig. 7. (a) Degradation of *average* device power shown with time after adjusting E_a and A for the curve computed, assuming that the failure region is at $T_{\rm fail}$. Otherwise, the curves are the same as in Fig. 6. (b) is the same as (a) but runs with a lower baseplate temperature of 180 °C instead of 200 °C. The thin dash-dotted line shows the 10% power degradation point.

Two temperatures and not three are needed to extract E_a' and A' because it is known that there is only one activation energy in the modeled degradation rate. A few test cases were run with a third temperature to verify this.

Simulations where the attempt to hold $T_{\rm fail}$ constant was done by adjusting gate voltage instead of increasing $T_{\rm base}$ are reported on last, because of a complicating factor. This is complicated by the fact that the proper local power adjustment factor depends on local transconductance (G_m), which may or may not degrade. Two different ways for the device to degrade were examined so that it would be known if this was an important consideration. In the first scenario (Scenario 1) investigated, the device has a local transconductance $(G_{m,\rm local})$ that is initially uniform and also does not drop with time. Degradation in this case is instead assumed to be due to a locally varying threshold voltage shift. In this case, adjusting $V_{\rm GS}$ simply adds the same value everywhere to $I_{\rm DS,local}$ and therefore also adds the same amount of power to the local power everywhere in the device. In the second scenario (Scenario 2), the device degrades by the reduction of $G_{m,\rm local}$, but local threshold voltage remains fixed, and it is also assumed that the entire $V_{\rm GS}-G_{m,\rm local}$ curve for all $V_{\rm GS}$ (at least near the $V_{\rm GS}$ of interest) has degraded by the same percentage. In this case, a small change in $V_{\rm GS}$ will everywhere *multiply* the $I_{\rm DS,local}$ and, therefore, the local power by the same factor. Effectively, degraded regions have less power recovery when $V_{\rm GS}$ is adjusted under Scenario 2 than under Scenario 1. Either way, degradation is measured by monitoring the power drop at the initial gate potential and is equivalent experimentally to periodically stopping the test to briefly return the gate potential to its original value to monitor degradation and then back to resume the test without this affecting the device.

TABLE I
EXTRACTED E_a' AND A' ESTIMATES WHEN POWER IS HELD CONSTANT BY ADJUSTING $V_{\rm GS}$ FOR SCENARIO 1

R_{th} for T_{base} =180 °C run (K·m / W)	R_{th} for T_{base} =200 °C run (K·m / W)	E_a' (eV)	A'	T_{fail} for T_{base} = 180 °C run (°C)	T_{fail} for T_{base} = 200 °C run (°C)
0	0	1.250	6.10×10^{9}	180	200
0.015	0.015	1.613	4.33×10^{11}	243	263
0.03	0.03	2.023	3.08×10^{13}	306	326
0.04245	0.04530	1.526	1.17×10^{8}	358.3	390.3
0.045	0.045	2.478	2.19×10^{15}	369	389

TABLE II
EXTRACTED E_a' AND A' ESTIMATES WHEN POWER IS HELD CONSTANT BY ADJUSTING $V_{\rm GS}$ FOR SCENARIO 2

R_{th} for T_{base} =180 °C run (K·m / W)	R_{th} for T_{base} =200 °C run (K·m / W)	E_a' (eV)	A'	T_{fail} for T_{base} = 180 °C run (°C)	T_{fail} for T_{base} = 200 °C run (°C)
0	0	1.250	5.78×10^{9}	180	200
0.015	0.015	1.613	4.11×10^{11}	243	263
0.03	0.03	2.023	2.92×10^{13}	306	326
0.04245	0.04530	1.527	1.11×10^{8}	358.3	390.3
0.045	0.045	2.479	2.08×10^{15}	369	389

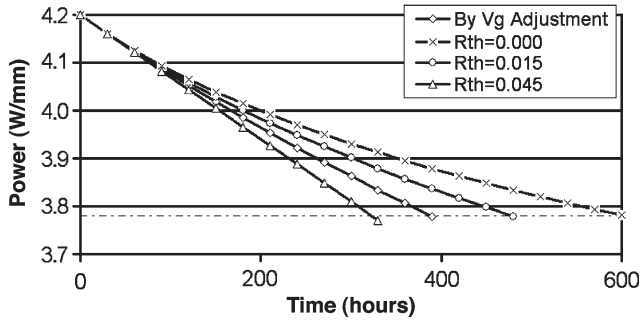

Fig. 8. Results for several guesses for $R_{\rm th}$ and for using $V_{\rm GS}$ adjustment to keep the power constant. *All are for the same device* with a starting baseplate temperature of 200 °C. The thin dash-dotted line shows the 10% power degradation point.

One advantage of this method is that the baseplate temperature is not adjusted, and $R_{\rm th}$ is not needed during the life test. $R_{\rm th}$ is still needed to extract E_a' and A', and the choice of $R_{\rm th}$ is still critical for correct data. Extracted E_a' and A' are shown in Tables I and II, and values were found to agree by better than 1 meV and 10%, respectively, between Scenarios 1 and 2 for the same $R_{\rm th}$; these differences are not significant.

Finally, in Fig. 8, the same device under the same starting conditions was simulated with either $T_{\rm base}$ adjustment with an assumed $R_{\rm th}$ or $V_{\rm GS}$ adjustment to keep average power constant. In practice, $R_{\rm th}$ is not an exactly known parameter, and it is common in a practical life test to assume a fixed value for $R_{\rm th}$ for the entire test. For higher $R_{\rm th}$ values, the baseplate is forced to greater temperatures to keep the calculated value of $T_{\rm fail}$ constant, and this is why the degradation rate of the devices is faster for these runs. For $R_{\rm th} = 0.045$, the degradation rate *accelerates* slightly with time despite the exponential decay expected from (1) because $R_{\rm th}$ is too high and the modeled temperature profiles (not shown) increase with time everywhere, with $T_{\rm base} = 218.9$ °C by the end of the test. Table III shows

TABLE III
EXTRACTED E_a' AND A' ESTIMATES FOR VARIOUS ASSUMPTIONS OF $R_{\rm th}$. IN ALL CASES EXCEPT FOR $R_{\rm th} = 0$, BASEPLATE TEMPERATURE IS ADJUSTED IN AN ATTEMPT TO HOLD $T_{\rm fail}$ CONSTANT. FOR ALL SCENARIOS, THE INITIAL "CORRECT" VALUES USED IN THE POWER DEGRADATION COMPUTATIONS FOR E_a AND A ARE 1.5 eV AND 2×10^8. THE FOURTH RUN DOES SO MUCH BETTER THAN THE REST BECAUSE, IN THAT CASE, THE KNOWN $R_{\rm th}$ FROM THE MODEL WAS USED IN THE ESTIMATION OF $T_{\rm fail}$. THE REGION MODELED AS FAILING IS THE CENTER OF THE BOTTOM OF THE GATE

R_{th} for T_{base} =180 °C run (K·m / W)	R_{th} for T_{base} =200 °C run (K·m / W)	E_a' (eV)	A'	T_{fail} for T_{base} = 180 °C run (°C)	T_{fail} for T_{base} = 200 °C run (°C)
0	0	1.264	5.21×10^9	180	200
0.015	0.015	1.607	2.84×10^{11}	243	263
0.03	0.03	1.989	1.47×10^{13}	306	326
0.04245	0.04530	1.526	1.30×10^8	358.3	390.3
0.045	0.045	2.413	7.66×10^{14}	369	389

TABLE IV
EXTRACTED E_a' AND A' ESTIMATES FOR LIFE TESTS OF DIFFERENT DEVICES. THE "BASELINE" DEVICE IS 8×400 μm, 25-μm GATE PITCH, RUN AT 4.2 W/mm, WITH 350-μm SiC SUBSTRATE, AND LIFE-TESTED AT 180 °C AND 200 °C, WITH E_a AND A BEING 1.5 eV AND 2×10^8, RESPECTIVELY. ALL OTHERS ARE IDENTICAL TO THE BASELINE EXCEPT FOR THE DIFFERENCES LISTED HERE. FOR ALL, POWER IS HELD CONSTANT BY ADJUSTING $V_{\rm GS}$, ASSUMING THAT DEGRADATION PROCEEDS ACCORDING TO SCENARIO 2

Device		E_a'(eV)	A'	T_{fail} for T_{base} = 180 °C run (°C)	T_{fail} for T_{base} = 200 °C run (°C)
Baseline		1.527	1.11×10^8	358.3	390.3
2.8W/mm		1.518	1.32×10^8	289.9	317.1
175 um SiC thk.		1.525	1.20×10^8	330.3	360.1
2×400 µm		1.505	1.76×10^8	269.1	294.6
2×150 µm		1.504	1.77×10^8	257.9	282.6
E_a = 2.0 eV		2.035	9.52×10^7	358.3	390.3
35 µm pitch		1.521	1.20×10^8	335.9	366.2
"Complex initial power"		1.527	1.22×10^8	354.9	386.6

the results for E_a' and A'; it is shown that $R_{\rm th}$ greatly affects the extracted data. Fig. 8 allows for a comparison to Sozza *et al.* [4], where devices were stressed under constant power by $V_{\rm GS}$ adjustment (their Fig. 6). While a direct comparison cannot be made due to the fact that this is a different device under different conditions (this paper specifically focuses on larger devices than theirs with greater temperature variations within a device), it can be seen that most devices have a degradation rate that slows gradually with time as expected. It is also apparent that there can still be a large device-to-device variation in the degradation rate of nominally identical AlGaN/GaN HEMT devices, which makes a direct comparison difficult.

Table IV shows how the extracted E_a' and A' vary with variations in the tested device geometry and conditions, and can be used as a guide to the error introduced experimentally by ignoring the temperature variation in the device during a life test, assuming. In other words, E_a is predicted to be overestimated slightly, and A is underestimated significantly compared to the real values. As expected, variations that reduce the heating within the device, through either reduced power or reduced thermal resistance, will make the extracted parameters more accurate. This is particularly true for reducing the active area of the device. The "complex initial power" entry of Table IV is where the local initial power was set as $P(x, n, t) \propto T(x, n, t)^{-0.6}$ to account for the expected temperature dependence of local power in a new device under the bias conditions in place, as mobility and saturation velocity drop with increasing temperature [2]. This relation will change somewhat under different biases, for example, with the exponent increasing to ~0.9–1.0 under an open channel [2], [13]. As an example, the initial power for the 200 °C baseplate "baseline" device was 4.085 W/mm in the center and 4.473 W/mm at the farthest point, but with the average value still 4.2 W/mm. Accounting for this effect, the 180 °C and 200 °C devices were about 4° cooler in the center and lasted about 6% longer during the life test, but there was no significant effect on extracted energy.

TABLE V
E_a' AND A' FROM TEN LIFE TESTS AT 180 °C AND 200 °C ARE EXTRAPOLATED TO COMPUTE LIFETIME FOR 100 °C BASEPLATE. THE 200 °C BASEPLATE DEVICE FAILED AT 378 h AND THE 180 °C BASEPLATE DEVICE AT 1465 h AT 4.20 W/mm, AND 7430 AND 31 390 h AT 2.80 W/mm. ALL OF THE EXTRAPOLATED LIFETIMES (LAST COLUMN) SHOULD BE COMPARED TO A SIMULATION OF DEGRADATION OF THE SAME DEVICE BUT AT 100 °C BASEPLATE WHICH FAILED AT 1.50×10^6 h AT 4.20 W/mm

Rth for T_{base} =180 °C run (K m / W)	Rth for T_{base} =200 °C run (K m / W)	Power dissipation for lifetest (W/mm)	E_a' (eV)	A'	Extrapolated t_{fail} for T_{base} =100 °C
0	0	4.20	1.250	5.78×10^9	1.41×10^6
0.015	0.015	4.20	1.613	4.11×10^{11}	1.14×10^6
0.03	0.03	4.20	2.023	2.92×10^{13}	9.74×10^5
0.04245	0.04530	4.20	1.527	1.11×10^8	1.51×10^6
0.045	0.045	4.20	2.479	2.08×10^{15}	8.62×10^5
0	0	2.80	1.331	2.16×10^9	4.71×10^7
0.015	0.015	2.80	1.584	4.47×10^{10}	4.77×10^6
0.03	0.03	2.80	1.858	9.23×10^{11}	6.68×10^5
0.03925	0.04182	2.80	1.518	1.32×10^8	1.05×10^6
0.045	0.045	2.80	2.154	1.90×10^{13}	1.16×10^5

The same modeling process used for the life tests can be used to simulate the device life under operating conditions. In this case, the same degradation mode is assumed to be active, but with a lower baseplate temperature. It is also assumed that degradation does not depend directly on bias conditions or total dissipated power but only indirectly through the effect of changing temperature in (1). Table V compares lifetime calculated using E_a' and A' from life tests at 180 °C and 200 °C and compared to modeled lifetime at 100 °C baseplate, where degradation proceeds according to Scenario 2. It is shown that the extrapolated lifetime compares fairly well to the modeled lifetime, *if the power is the same for the life test as for the simulated operating conditions*. This is true even when E_a' and A' are off because the wrong $R_{\rm th}$ was used. When power is different for the life test versus the predicted usage, it is critical to use the right $R_{\rm th}$. The observations made in this paragraph were found to hold true even if fundamental changes are made to the model such as disabling the temperature dependence of the thermal conductivity or moving the region where $T_{\rm fail}$ is extracted far from the gate (in which case it was modeled so that both the failing region and the region for determining $R_{\rm th}$ were the same off-gate region). However, if a different region is measured to get $R_{\rm th}$ through error or limited spatial resolution of the measuring technique than is actually failing, then, of

course, E'_a will be off as discussed, and the previous statement does not apply.

IV. Conclusion

It can be seen that there is a modest error introduced in the values of E'_a and A' extracted from a life test from neglecting the spatial and variation over time of $R_{\rm th}$ and instead using the peak value. This is true even when using the same $R_{\rm th}$ extracted from the thermal model for the simulated life test. These errors are greatly compounded when $R_{\rm th}$ is not known and approximate values are used instead, highlighting the importance of getting this parameter and *its temperature dependence* right in a life test. Of course, it is impossible to know $R_{\rm th}$ without knowing exactly where the fail region is, and even then, there may be considerable uncertainty in this parameter. However, these errors can be minimized by careful modeling efforts and by careful measurement and, in general, will be much less for smaller devices.

It is shown that the error in E'_a and A' becomes a much greater problem for lifetime prediction specifically when the dissipated power is not the same for the life test as for the usage conditions. Also, it is seen that peak and average fail region temperature evolve differently depending on how the life test is performed (baseplate versus gate voltage adjustment), so that it is possible for this average temperature to stay relatively constant while the peak temperature changes considerably; an electrical test sensitive to this average temperature would be misleading.

We expect the same issues to be present in the RF device testing, because similar temperature profiles as discussed here have been shown experimentally for RF drive as for dc drive [14], and temperature is again an accelerating factor in degradation based on the same Arrhenius model (except that, typically, RF output power replaces $I_{\rm DS}$). However, RF life testing is commonly done by driving the devices to a set power saturation level and not to a set total power dissipation. As such, there is typically a different amount of power dissipation during the life testing than there is in the device during actual use, and so, based on our findings, errors in $R_{\rm th}$ are likely to be much more critical. We hope to extend this paper to allow simulation of RF measurements to test this hypothesis.

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